

ST330/30 Part 2
Electronics Technology
Student Workbook.

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SCANTEK 2000 - A division of LJ Technical Systems.

Written by: LJ Technical Dept

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Symbols Record Sheet

Draw the circuit diagram symbols that you come across while you study this module:

Resistor	Thermistor	Variable Resistor	Potentiometer	Preset Potentiometer
Joined Conductors	Crossing Conductors	SPST switch (normally open)	SPST switch (normally closed)	Switch (push to break)
Switch (push to make)	SPDT Switch	DPDT Switch	Light Emitting Diode (LED)	Diode
Cell	Battery (of cells)	Signal Generator	DC Power Supply	Amplifier
PNP Transistor	NPN Transistor	Thyristor	Electrolytic capacitor	Non-polarized capacitor
Light dependent Resistor	Schmitt Trigger	Lamp	Motor	Oscilloscope
Relay	Loud speaker	Bell	Buzzer	AND Gate
OR Gate	NOT gate	NAND gate	NOR gate	XOR gate
Op-amp	Photodiode	Field Effect Transistor	Phototransistor	Ground

Assignment 16 *Digital Electronics*

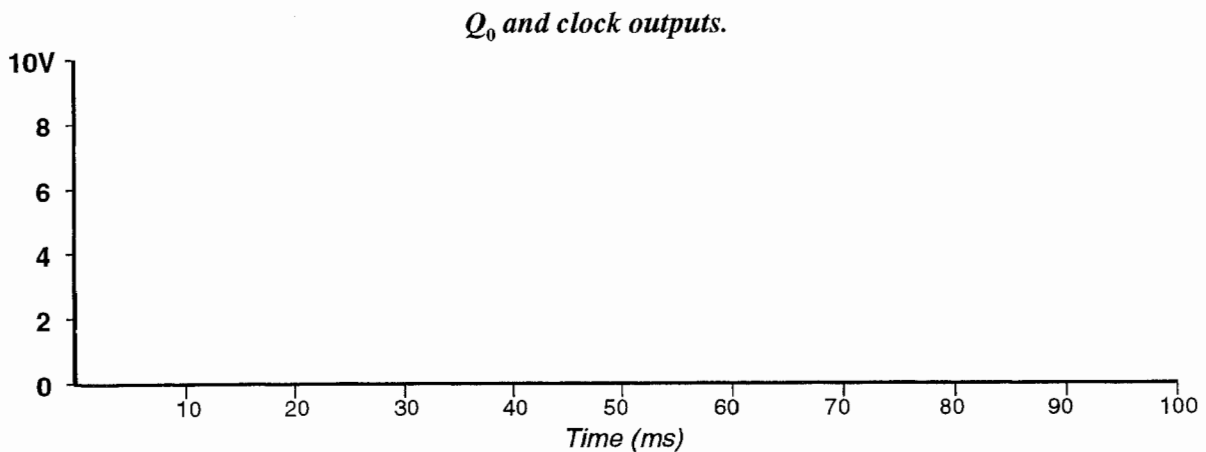
Complete 16.1 table showing the binary inputs for the seven segment display

Input				Output
I3	I2	I1	I0	Display
0	0	0	0	0
0	0	0	1	1
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

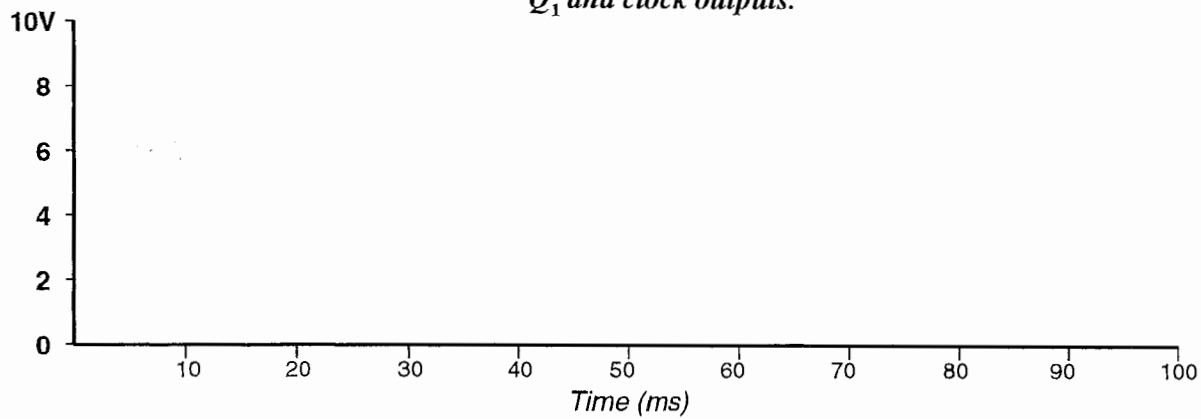
Table 16.1

Assignment 18 *Counter Sequencing*

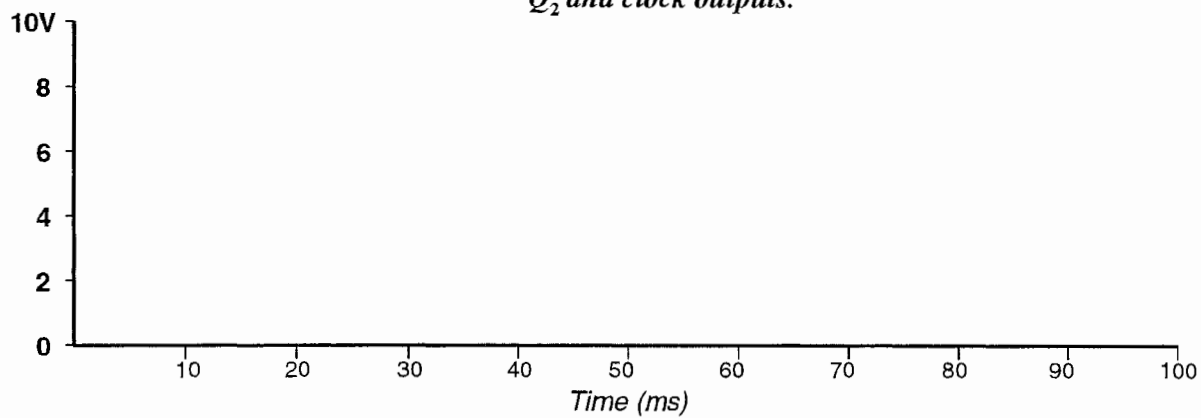
Draw the output signals on the chart that you see on the VLAB for the clock and Q_0 Q_1 Q_2 and Q_3 outputs.



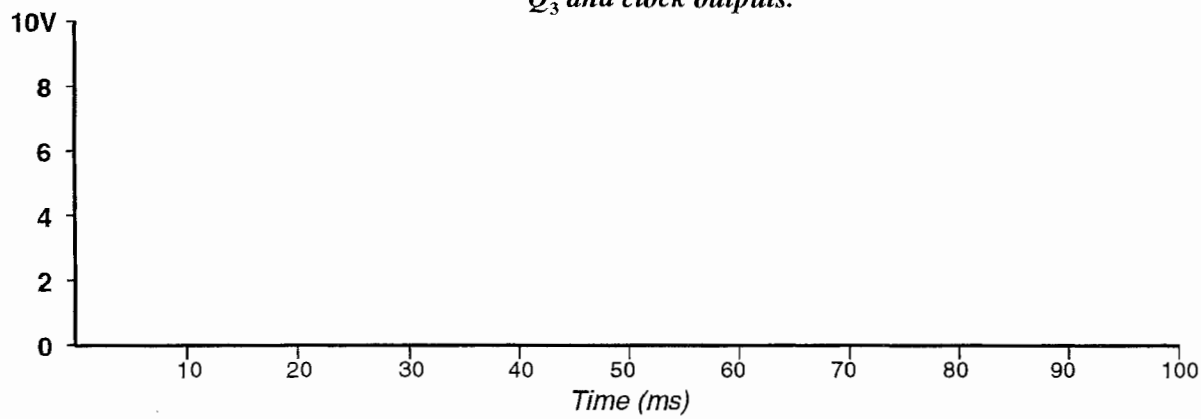
Q₁ and clock outputs.



Q₂ and clock outputs.



Q₃ and clock outputs.



Assignment 21 Logic Gates

Complete the truth tables, tables 21.1 and 21.2, for the AND and NOT gate.

Input		Output
I1	I0	Q0
0	0	
0	1	
1	0	
1	1	

Table 21.1 - AND gate

Input	Output
I0	Q0
0	
1	

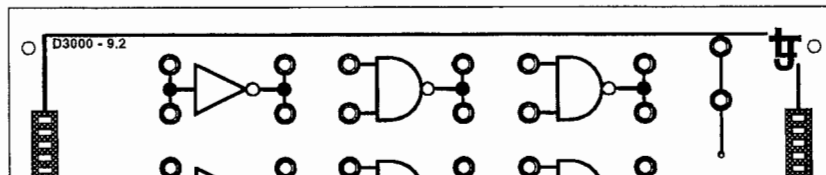
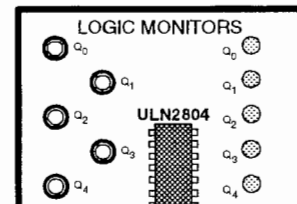
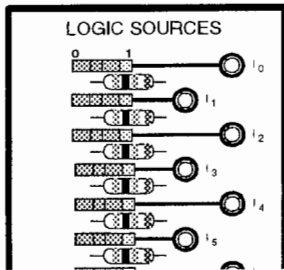
Table 21.2 - NOT gate

Complete the truth table, table 21.3 for the NAND gate.

Input		Output
I1	I0	Q0
0	0	
0	1	
1	0	
1	1	

Table 21.3 - NAND gate

Draw your NAND gate circuit in the space below (AND followed by a NOT).



Assignment 23 *OR, NOR Logic*

Complete the truth tables shown below.

Input		Output
I1	I0	Q0
0	0	
0	1	
1	0	
1	1	

Table 23.1 - OR gate.

Inputs			Output
I2	I1	I0	Q0
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 23.2 - 3 input OR gate.

Input		Output
I1	I0	Q0
0	0	
0	1	
1	0	
1	1	

Table 23.3 - NOR gate.

Assignment 24 *Combinational Logic*

Complete the truth tables shown below.

Input		Output
I1	I0	Q0
0	0	
0	1	
1	0	
1	1	

Table 24.1 - XOR gate.

Input		Output		Value
I1	I0	Q0	Q1	
0	0			
0	1			
1	0			
1	1			

Table 24.2 - Half Adder truth table.

Assignment 25 *It's All A Matter Of Logic*

Draw your circuit using logic symbols in the space below.

Assignment 27 *Decoding The Display*

Shade in the segments of the display which correspond to the lit LEDs.

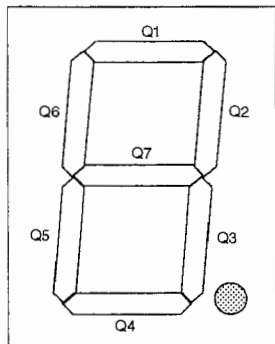


Diagram A

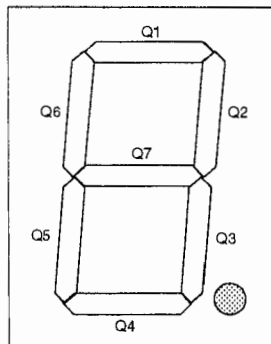


Diagram B

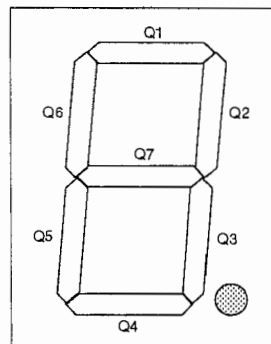


Diagram C

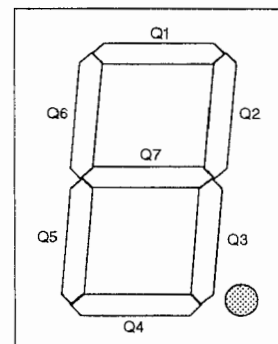


Diagram D

Assignment 29 *Electronic Dice Part 1*

Draw a block diagram for the Electronic Dice System below:

Draw a schematic diagram for your solution to the Electronic Dice System below: